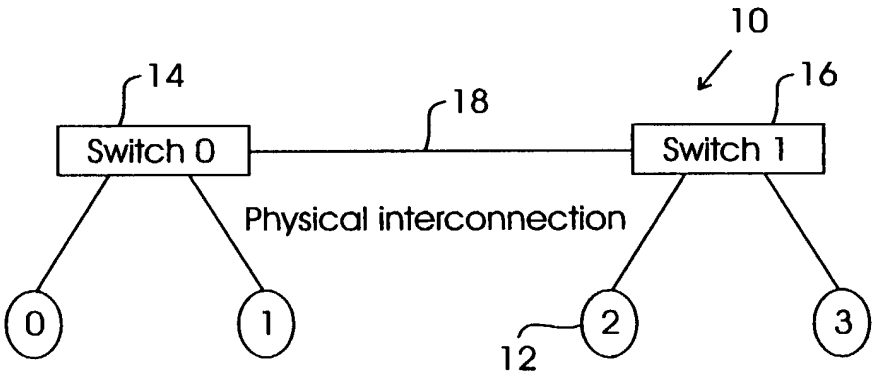

FIG. 1
PHYSICAL
SYSTEM

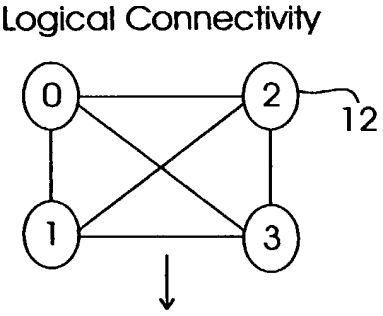

FIG. 2
LOGICAL
SYSTEM

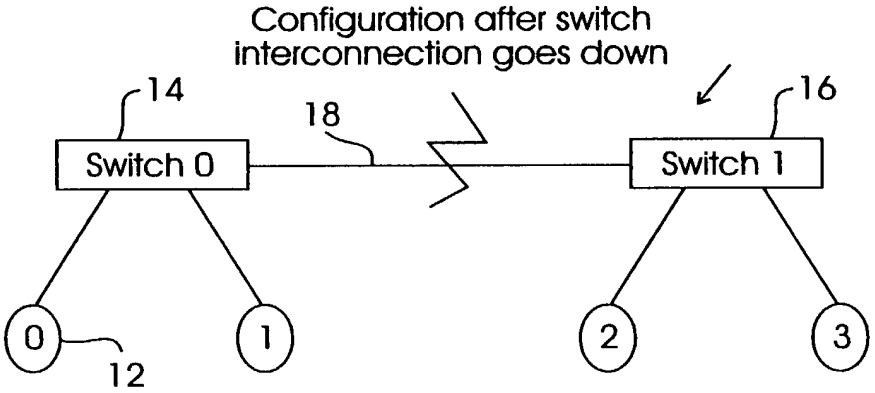

FIG. 3
SYSTEM WITH
BROKEN LINK

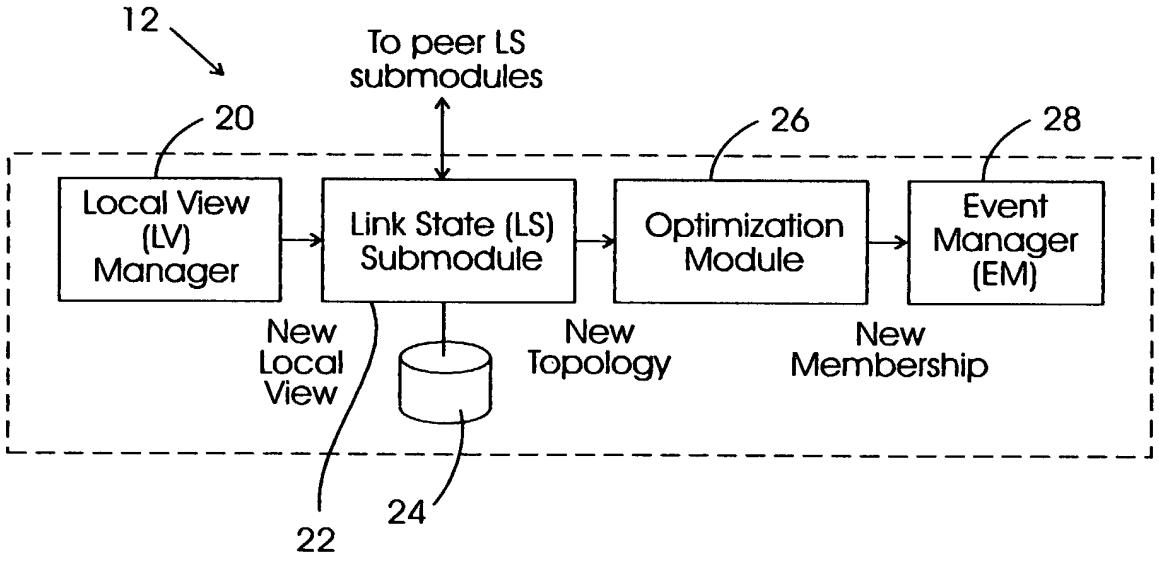

FIG. 4
NODE ARCHITECTURE

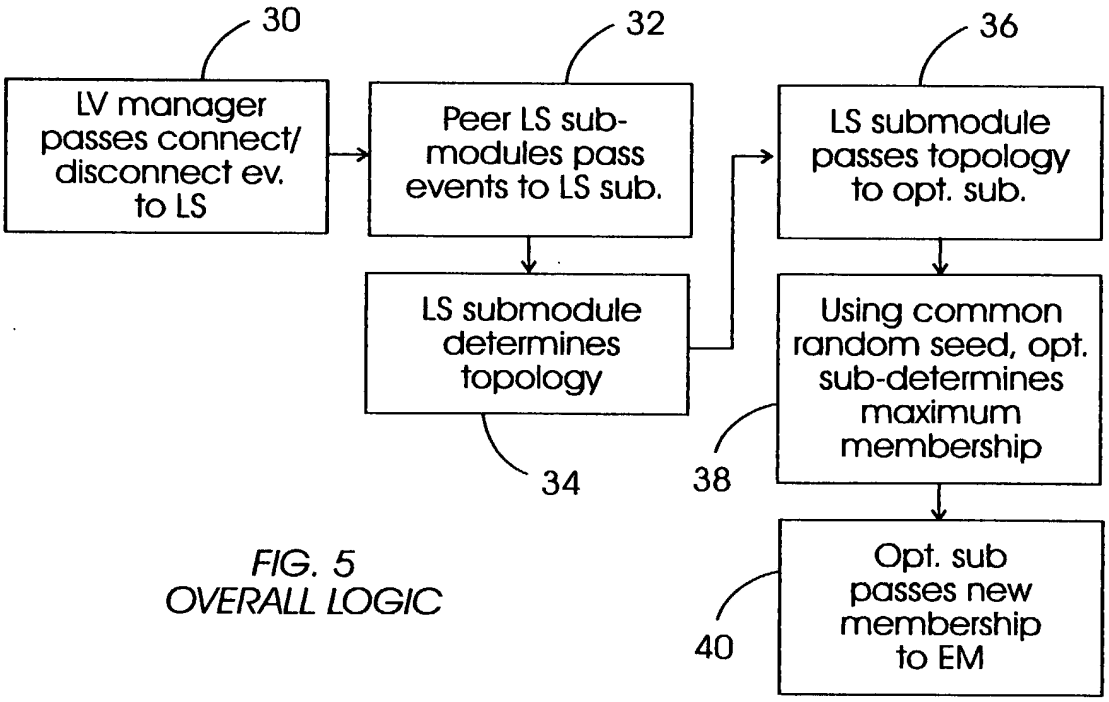

FIG. 5
OVERALL LOGIC

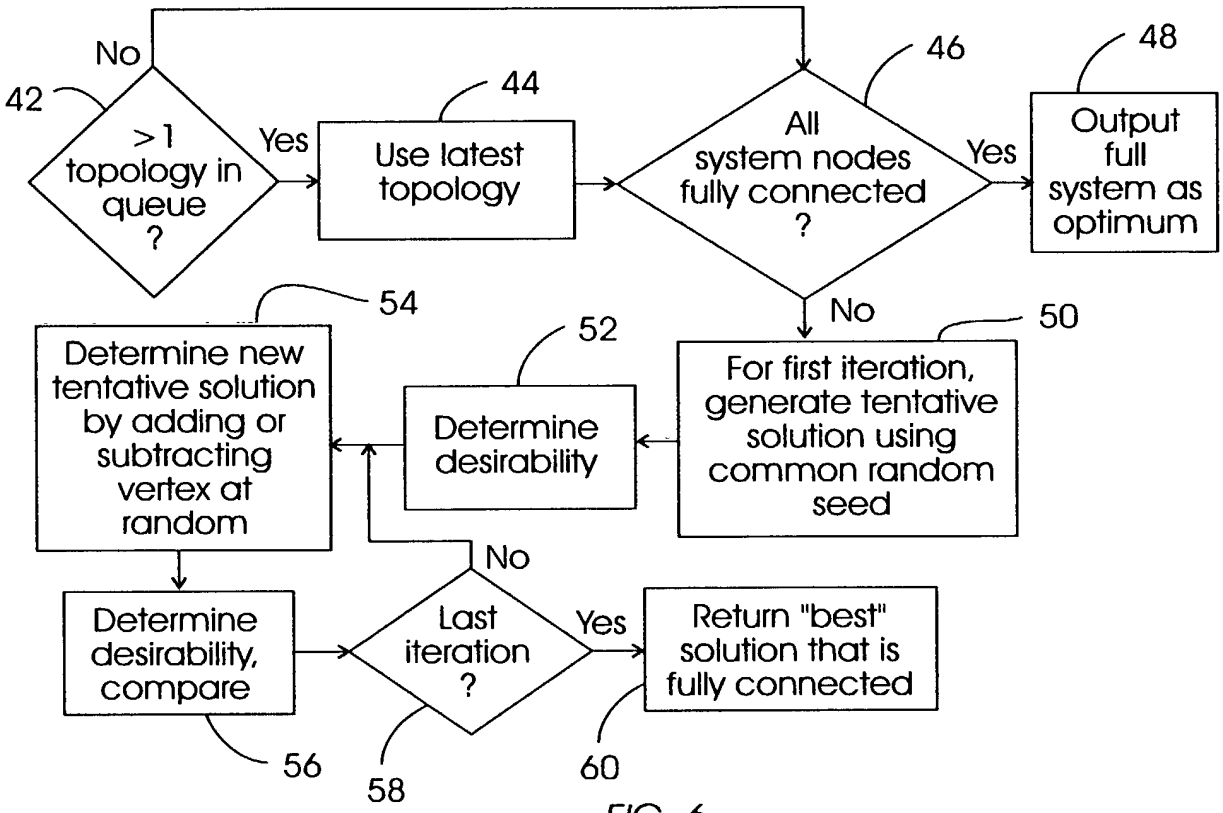

FIG. 6
OPTIMIZATION LOGIC

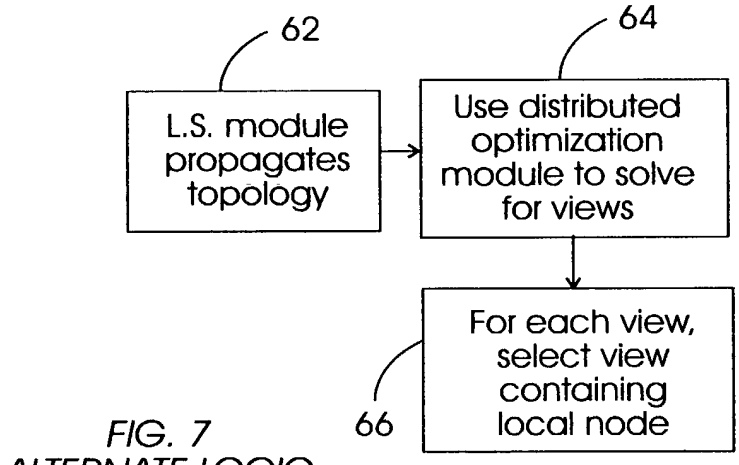

FIG. 7
ALTERNATE LOGIC